T-CREST

Time-predictable Multi-Core Architecture for Embedded Systems

EXECUTIVE Summary

New tools for designing time-predictable multicore systems that simplify the safety argument with respect to maximum execution time and substantially lower maximum execution times for safety-critical systems.

PROJECT Objectives

Research and develop novel solutions for time-predictable multi-core and many-core system architectures utilising time-predictable resources (processor, interconnect, memories, etc) designed to accomodate WCET analysis and that optimize WCET performance.

MARKET Motivation

Standard computer architecture is driven by the following paradigm: make the common case fast and the uncommon case correct. This leads to architectures where the average-case execution time is optimized at the expense of the worst-case execution time (WCET). Modelling the dynamic features of current processors, memories, and interconnects for WCET analysis often results in computationally infeasible problems. The bounds calculated by the analysis are thus overly conservative.
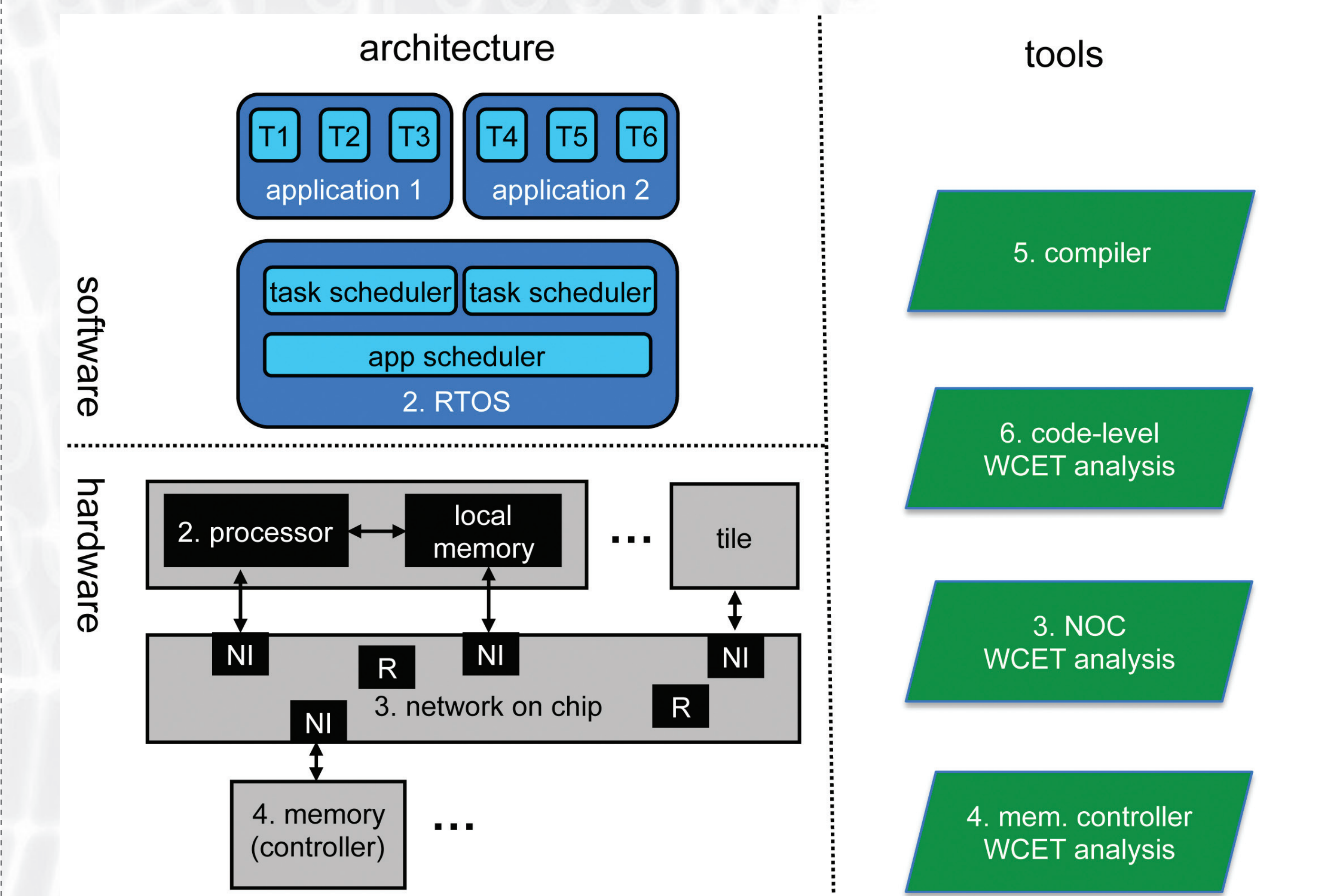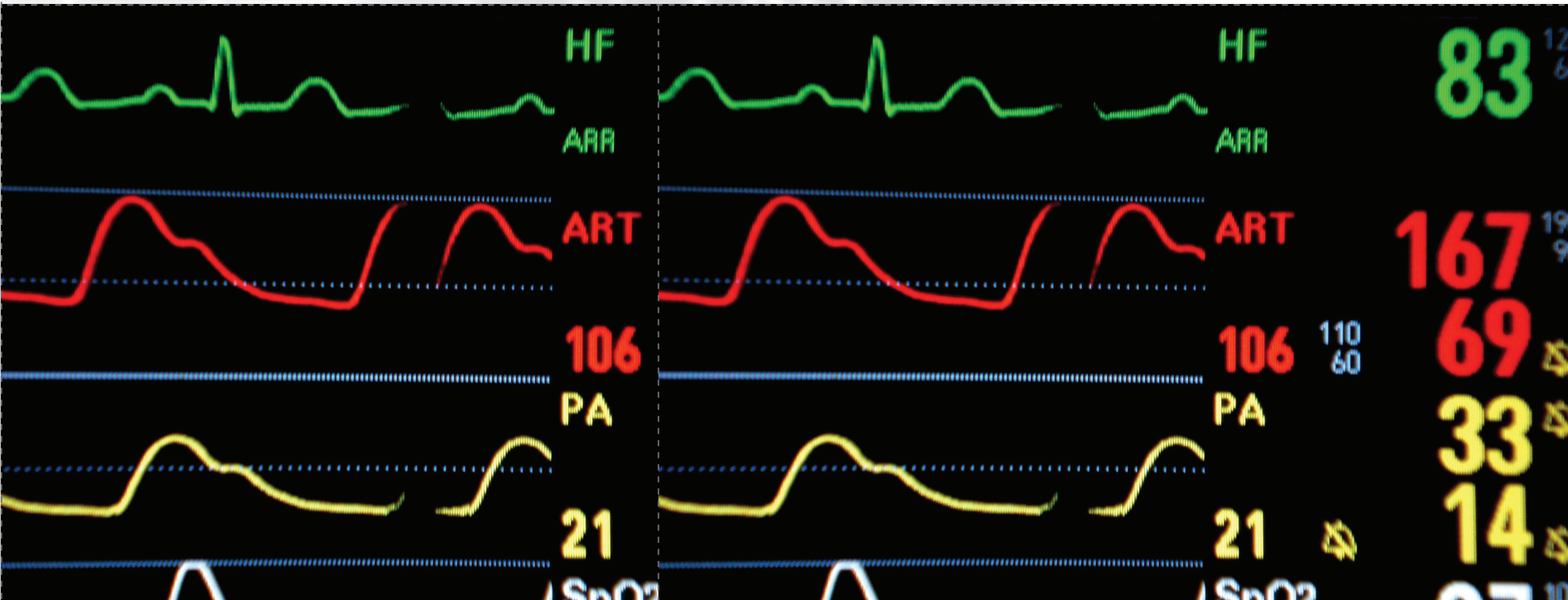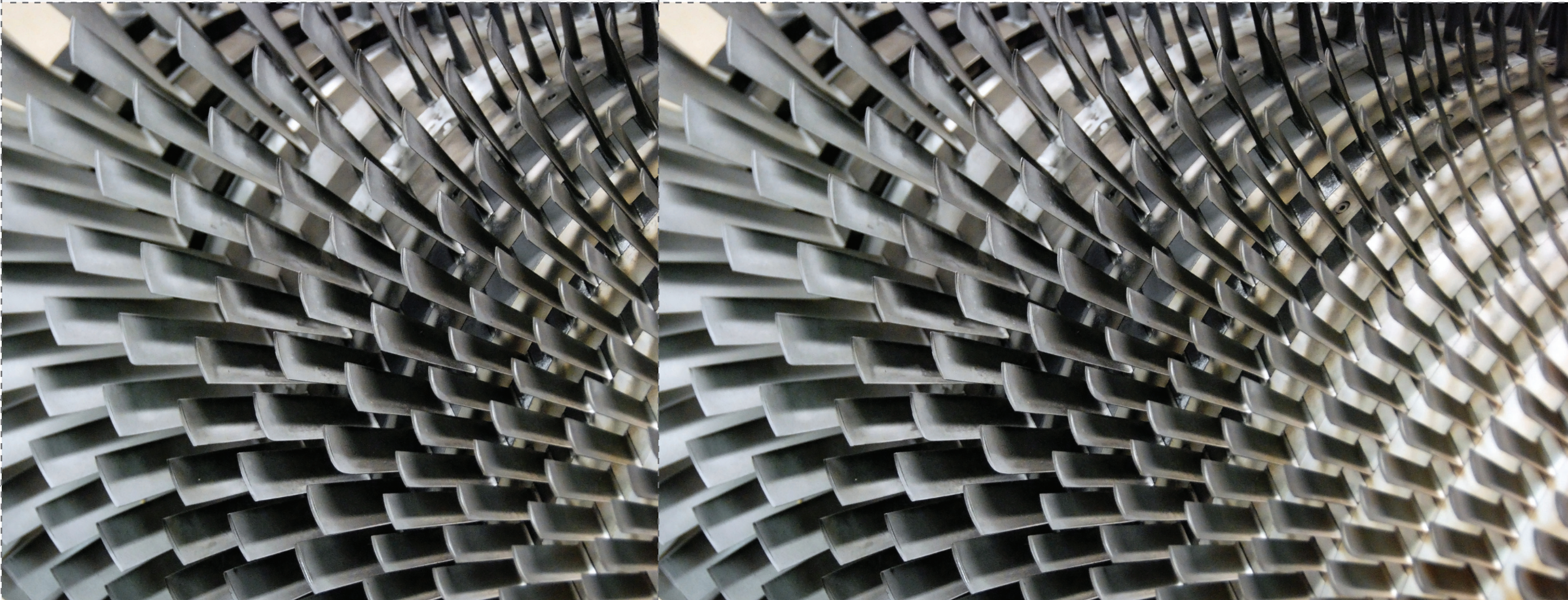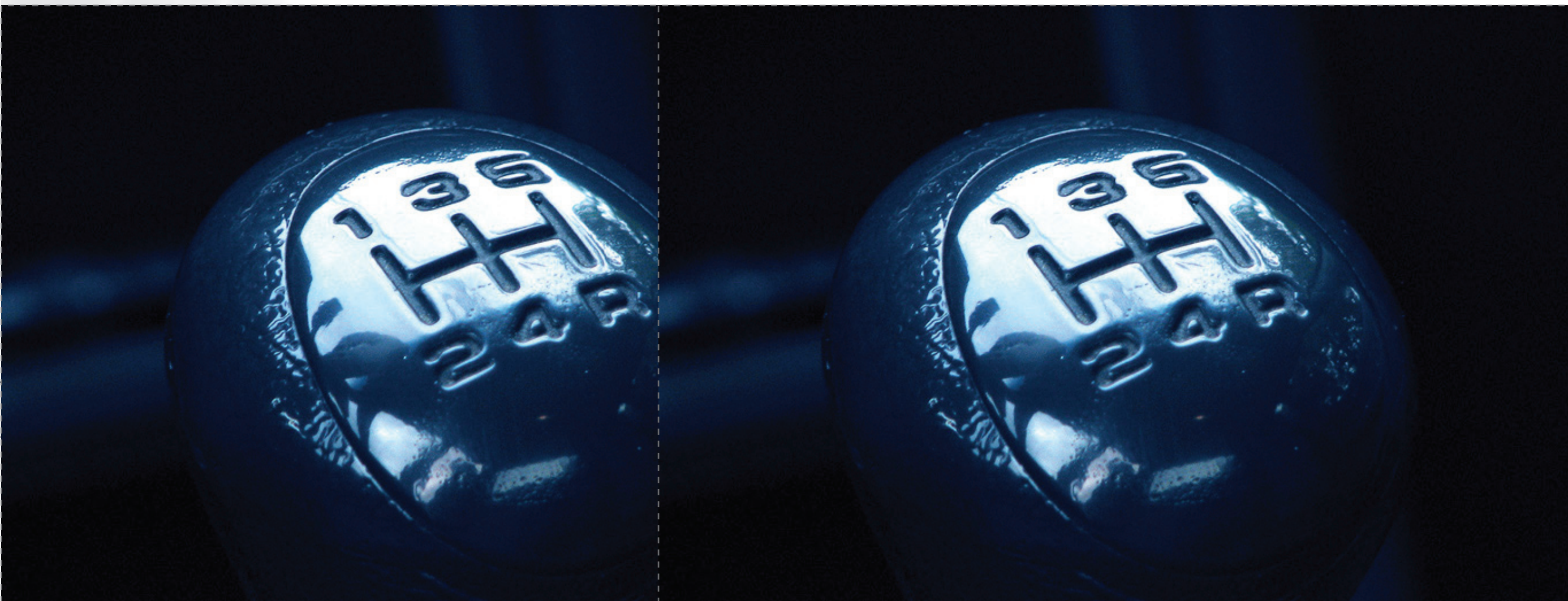
For real-time systems, we need a dramatic change to designing computer architectures using a new paradigm: make the worst-case fast and the whole system easy to analyze. T-CREST seeks to develop new computer architectures where predictable timing is a first-order design factor.

Technical Innovations

Research and technology development topics addressed in the project:

> Time-predictable processor for optimizing WCET and tightening the WCET bound

> Asynchronous time-predictable Network-on-Chip interconnect

> Time-predictable memory hierarchy with caches organized to speed-up exection time and provide tight WCET bounds

> Compiler infrastructure with WCET aware optimization methods and timing models to adapt to hardware behaviour

> WCET analysis techniques to exploit the time-predictable architecture

> FPGA prototypes able to execute use cases from industry

Technology advancements are driven by industrial requirements and validated in application development by industry leading partners.

architecture

| software | T1 | T2 | T3 | T4 | T5 | T6 |

application 1   application 2

task scheduler   task scheduler

app scheduler

2. RTOS

hardware

2. processor ↔ local memory ··· tile

NI   R   NI   NI

NI

3. network on chip   R

4. memory (controller) ···

3. network on chip

tools

5. compiler

6. code-level WCET analysis

3. NOC WCET analysis

4. mem. controller WCET analysis

T-CREST

PROJECT CONTACT	**DURATION**
Martin Schoeberl	36 months
INSTITUTION	**COMPLETION**
Denmark Technical University	August 2014
EMAIL	**TOTAL COST**
masca@imm.dtu.dk	3.6 M€
WEBSITE	
www.t-crest.org	